NEWS RELEASE

Forte Design Systems Announces SystemC Synthesis Success with Fujitsu Microelectronics Europe

Forte's Cynthesizer Deployed for New Graphics Processor Design to Reduce Project Cycle, Provide Flexibility for Architectural Exploration

SAN JOSE, CALIF. –– August 3, 2009 –– Forte Design Systems announced today that Fujitsu Microelectronics Europe (FME) of Frankfurt, Germany, used its Cynthesizer™ SystemC synthesis software to successfully implement a subsystem of FME's new graphics processor unit.

This follows an earlier announcement by FME's parent company Fujitsu Microelectronics Limited on the selection of Cynthesizer for its application specific integrated circuit (ASIC) reference flow. Fujitsu Microelectronics further confirmed that the register transfer level (RTL) code created by Cynthesizer met its stringent RTL sign-off requirements for users of its foundry services.

FME's newly introduced MB86298 OpenGL ES2.0 graphics processing unit offers high-performance 3D-rendering for automotive and industrial applications that use an overlay of computer graphics and video data. The rendering engine incorporates a programmable unified shader entirely designed and implemented in high-level SystemC using Cynthesizer. The pipeline structure of the shader unit was configurable to use high-level geometry, color and lighting algorithms for full-scene anti-aliased (FSAA) image generation.

"Forte's Cynthesizer gave us the flexibility to make architectural changes late in the project without having to rip up and redo hand-coded RTL," says Raimund Soenning, Manager Hardware Development at FME. "As a result, we were able to explore several different architectures and algorithms to find the one that met our challenging performance and area targets."

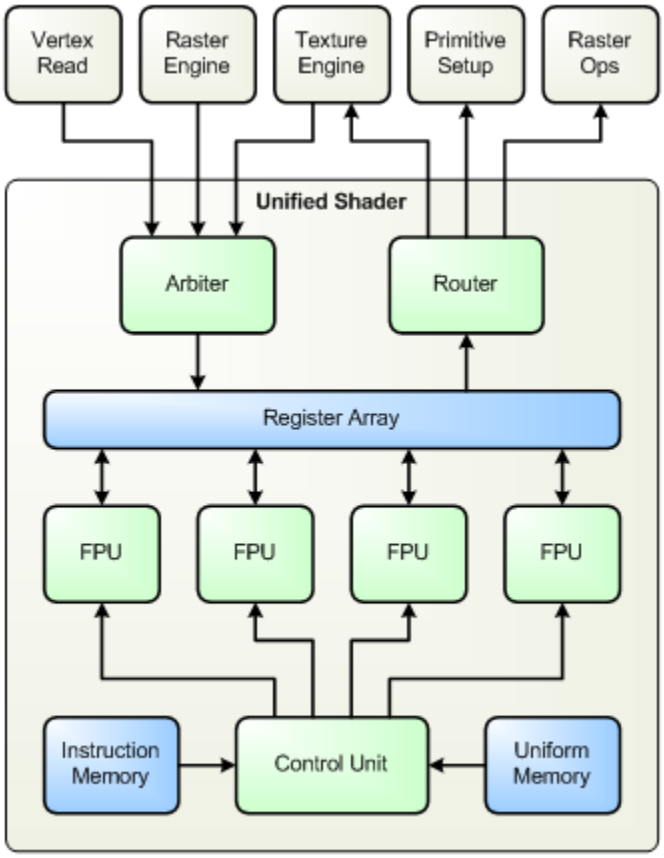
Implementing the Graphics Processor Using Cynthesizer

The shader is a custom floating-point processor that executes the OpenGL ES 2.0 shading language for user-specific operations on vertices and fragments. The design was implemented in 24 engineer-months using Cynthesizer – significantly less time than it would have taken in RTL Verilog.

The project was broken into two main subsystems: a controller and several arithmetic units, each with more than 12 sub-blocks connected in a structural hierarchy. The design team implemented the hierarchy and interconnect in synthesizable SystemC, with most of the verification performed using high-level SystemC code to avoid costly RTL simulation runs. A hierarchical construction methodology of the behavioral SystemC similar to the way these tasks would be performed using RTL hardware design languages Verilog and VHDL allowed the validation of synchronization and resource sharing using high-speed behavioral simulations.

A controller subsystem implemented the instruction processing and branching functionality and controlled the movement of data into and out of multiple arithmetic units. This included blocks such as instruction decoders, routers, memory arbiters and others. The team was able to write these control-dominated parts of the design at a high level of abstraction and used Forte's CynWare™ point-to-point interface intellectual property (IP) for point-to-point communication between the submodules of the processor. By taking advantage of its built-in flow control and stalling capabilities, the control-dominated parts of the processor were easier to write than if they were hand-coded in RTL. Each element of the processor runs at full speed when data is available for processing without the designers micro-managing the latencies of each block or manually inserting synchronization logic.

The arithmetic subsystem contains a number of identical arithmetic units that implement floating point vector operations using the Forte's CynWare cynw_float class and trigonometric, square root, and exponential functions with Forte's sc_fixed compatible cynw_fixed class. By taking advantage of the parameterized flexibility of the cynw_float class, the team was able to adjust the floating point precision to explore alternative architectures as the project evolved. Doing this in RTL code would have required extending the project schedule or settling for a sub-optimal architecture.



During the course of the project, Forte implemented a floating-point multiply-accumulate algorithm to allow the design team to meet performance goals that required two-cycle floating-point multiply-accumulate operations at 266 MHz clock rate.

"Overall, we were pleased with the experience using Cynthesizer for this challenging design," concludes Roland Richter, senior design engineer at FME. "We found it relatively easy to achieve initial RTL code and optimize the results. Without Cynthesizer, the design would have taken much more time and manpower to build by hand in RTL code. In fact, we question whether it could have been completed within our product delivery window at all."

About Forte Design Systems

Forte Design Systems is a leading provider of software products that enable design at a higher level of abstraction. Its innovative high-level synthesis technology allows design teams creating complex electronic systems from algorithmic designs using ASICs, FPGAs, and SoCs to significantly reduce their overall design and verification time. Forte is headquartered at 100 Century Center Court, San Jose, Calif. 95112. For more information, visit www.ForteDS.com.

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